AF/ 2818

PATENT
Docket No. 606402014400

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:	
Shuichi TAKAHASHI *et al.*	Examiner: Dao H. Nguyen
Serial No.: 10/696,580	Group Art Unit: 2818
Filing Date: October 30, 2003	Conf. No. 7212
For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE	

Please Enter this paper.
Thanks,
DN
06/19/2006

RESPONSE UNDER 37 CFR 1.116

M/S AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Action mailed March 10, 2006, please reconsider this application in light of the following remarks:

REMARKS

Claims 1, 5 and 6 have been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,537,877 (Ishida). Applicants respectfully traverse this rejection.

In the amendment filed December 27, 2005, applicants amended claim 1 to state that some but not all of the memory transistors are connected with corresponding bit lines by corresponding metal plugs of the one of the insulating layers. Applicants explained that in the claimed memory device, the connection pattern between the memory transistors and the bit lines is permanent and cannot be changed because there is no way to add or delete the metal plugs once the claimed memory device is manufactured. In other words, the claimed memory device provides a read only memory (ROM). On the other hand, Ishida's SRAM is composed of a